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# RRB - JE

# ELECTRONICS

## Railway Recruitment Board

Volume - 8

## Computer Fundamentals

SIERRA
INNOVATIONS

# CONTENTS

# BASICS OF COMPUTER ARCHITECTURE

## THEORY

## INTRODUCTION

**COMPUTER ARCHITECTURE :**

An architecture concern with the structure seen by the user and their behaviour.

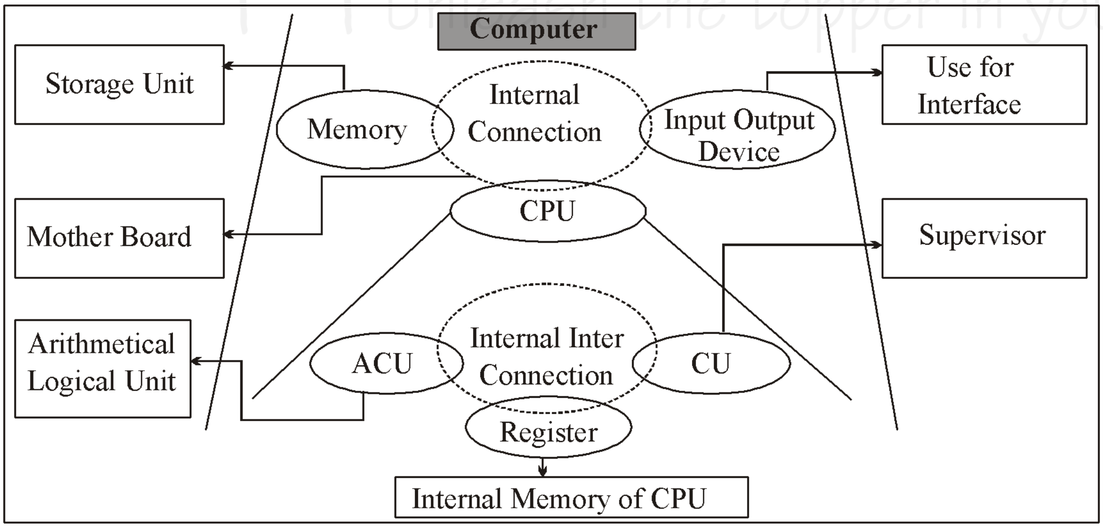
An architectural attributes includes machine instruction, addressing modes, data type, no of bits used for each data.

## 1.1 COMPUTER ORGANIZATION

An organization concern with the internal oparational unit of the system and the way they are inter connected to form the computer system.

Organizational attributes includes control signals, input output techniques.

Computer is not a stand alone device.



## 1.2 COMPUTER GENERATION

The divison of computer system into generation is determined by the device technology, system architecture, processing mode and languages used.

### 1.2.1 First Generatin (1938 – 1953) :

IN which we use the ***Vaccum Tubes*** it is a first electronic component.

The first electronic computer is devloped in first generation namely.

***ENIAC*** (Electronic numerlcal integrator and calculator or computer)

In which we use the ***machine language.***

There is ***no operating system*** available in first generation.

In which the airthmetic is done by bit by bit fixed point basis, as in aripple carry addition which uses ***a single full adder and one bit of carry flag.***

In the first generation we also use the first stored programmed computer ***EDVAC*** (Electronic discrete variable automatic computer)

### 1.2.2 Second Generation :

In the second generation we use the transistors.

The first transistorzed digital computor is ***TRADIC***.

In which we use the assembly language and high level programming language.

The first high level language is ***FORTRAN*** (Formula Translation)

In second generation we also use the algorithmic language lipe ***ALGO*** (Algorithmic language)

In which we use the ***Batch processing.***

In which we also use the inter changeable disk packs for storing the data.

### 1.2.3 Third Genration :

In the third generation we use the IC's (Integrated circuit)

***In which IC's :***

- ***SSI*** (Small Scale Integration)
- ***MSI*** (Medium Scale Integration)
- ***LSI*** (Large Scale Integration)

In which we use the high leme programming language.

Intelligent compiler and virtual memory and memory hierarchy was introduced in third generation.

In which we use the multiprogramming and timesharing.

### 1.2.4 Fourth Generation :

In which we use a technique ***VLSI*** (Very Large Scale Integrated Circuit)

In which we use the multiprocessor and preal time operating system.

In the fourth generation we also use the ***RDBMS*** (Relational data base management system)

8085 microprocessor is also introduced in first generation.

## 1.3 FLYNN'S CLASSIFICATION

According to flynn's digital computer may be classified into four categories accoraing to multiplicity of instruction and data streams.

An instruction stream is a sequence of instructions as executed by the machine.

A data stream is a sequence of data including input, partial or temporary results, called for by the instruction stroam.

***According to Flynn's category of Computer :***

- ***SISD*** (Single instruction single data)
- ***SIMD*** (Single instruction multiple data)
- ***MISD*** (Multiple instruction single data)
- ***MIMD*** (Multiple Instruction multiple data)

### 1.3.1 SISD (Single Instruction Single Data) :

It execute only one instruction at a time.

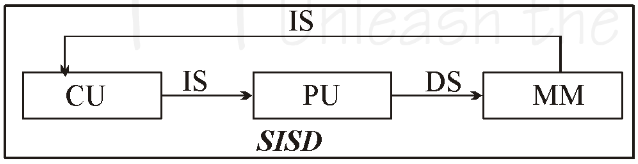
It is a uniprocessor system.

CPU is partitioned int as

***CPU :***

- Control unit (Unicu)
- Airthmetical Logical Unit (Uni Airthmetical Logical Unit)
- Register (More than one)

***Example :*** Von neuman Architecure



CU = control unit

PU = Processing Unit

MM = Memory module

IS = Instruction Stream

DS = Data stream.

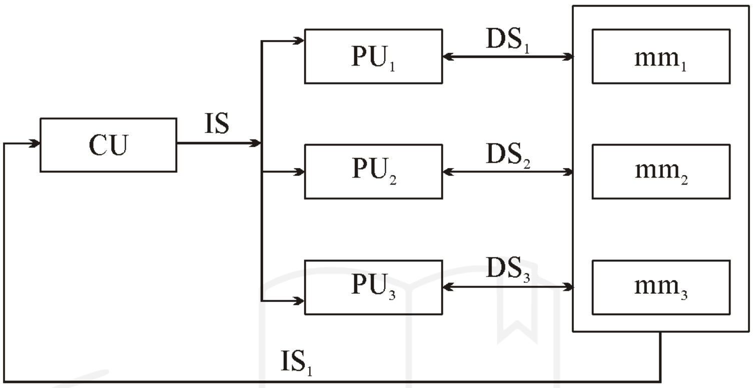
### 1.3.2 SIMD (Single Instruction Multiple Data) :

***CPU :***

- CU (One CU)
- Airthmetical Logical Unit (More then one)
- Register (More than one)

It perform only one operation at different 2-Data.

| $ALU_1$ (PU) | $ALU_2$ ($PU_2$) | $ALU_3$ ($PU_3$) |
|---|---|---|
| Add (10, 20)<br>Different-2 data<br>Single Operation | Add (30, 40) | Add (50, 60) |



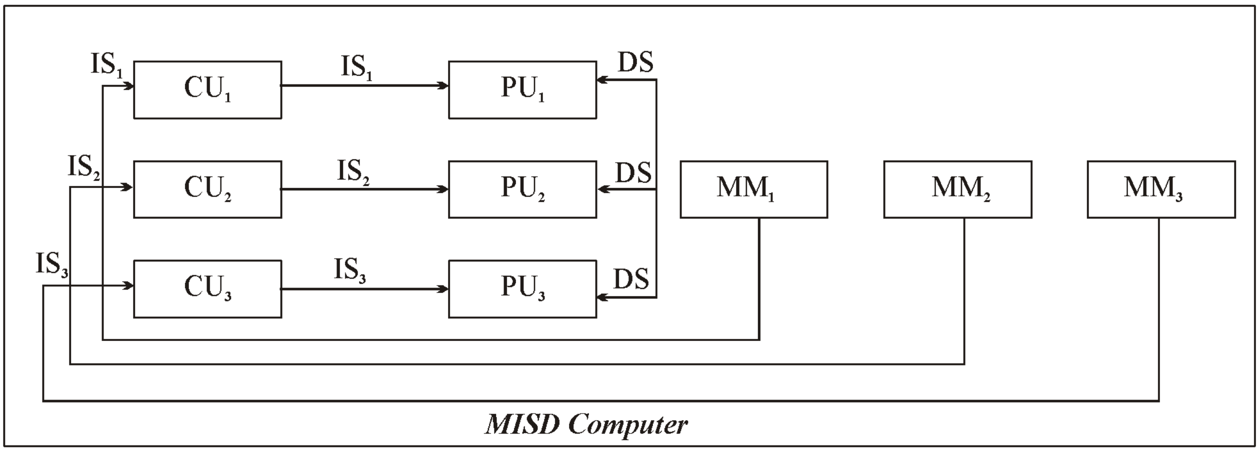
Single instruction and multiple data is not used for desktop application it is used for application specific process.

### 1.3.3 MISD (Multiple Instruction Single Data) :

***CPU :***

- CU (More then One)
- Airthmetical Logical Unit (More then one)
- Register (More than one)

Different-different operation are perforemed on single data.



*MISD Computer*

No computer is base on this module.

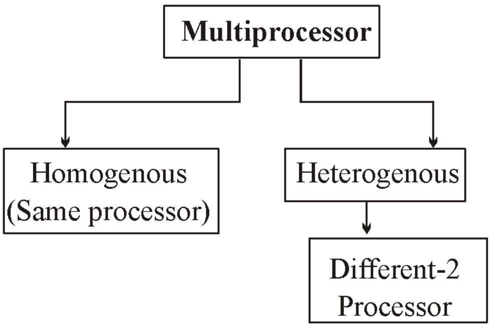
### 1.3.4 MIMD (Multiple Instruction Multiple Data) :

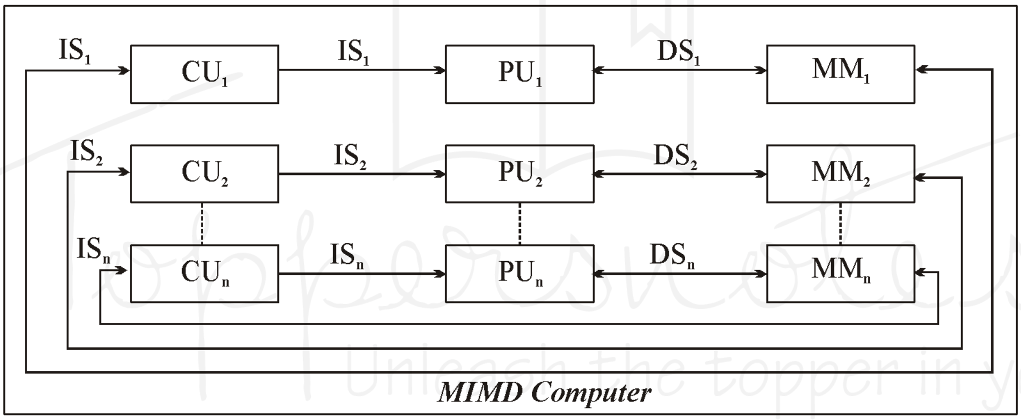
*CPU :*

- CU (One CU)
- Airthmetical Logical Unit (More then one)
- Register (More than one)

It perform only one operation at different 2-Data.

***In which we have multiprocessor :***

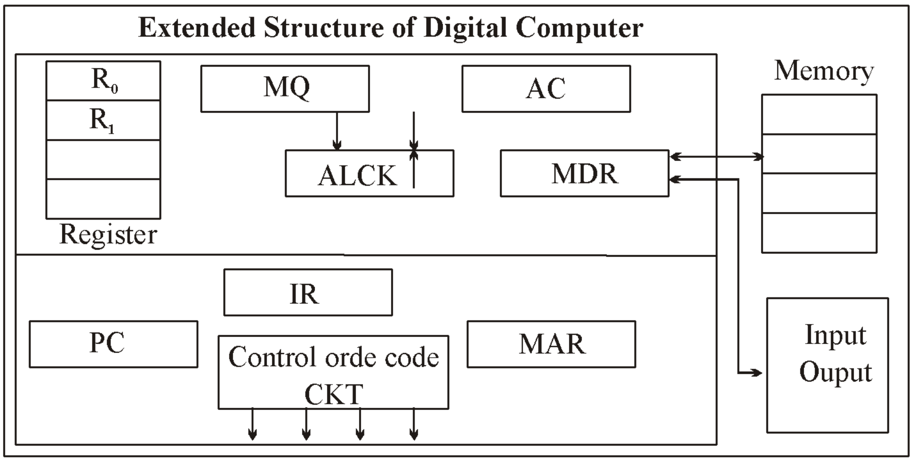




*MIMD Computer*

## 1.4 EXTENDED STRUCTURE OF DIGITAL COMPUTER

**Extended Structure of Digital Computer**



***(i) Program counter :***

It holds address of the next instruction to be fetched from memory.

***(ii) Memory Address Registor (MAR) :***

It holds the address of the memory location used for either readwrite operation.

***(iii) IR (Instruction Register) :***

It holds the Instruction currently being executed by CPU.

Memory data register orbremory buffer register or data register.

It holds the data either to be written into memory or read from the memory.

***(iv) MQ (Multiplier Quaient) :***

Contain order of result.

***(v) AC (Accumlator) :***

They are the registers holds either intermediate result or temprory data or one operand of the operation.

($R_0$, $R_1$, $R_2$-------$R_n$) → General Purpose Register.

***(vi) AL–CKT :***

Airthmetical logical CKT. It program the airthmetic and logical operation.

***(vii) Control CKT :***

It supervise each end every activity in the digital system.

***(viii) Register :***

- GPRS (General purpose registors)

  $R_0$, $R_1$, $R_2$---------$R_n$.

- SPRS (Special Purpose Registors)

  PC, IR, MAR< MBR, MQ, Accumlator.

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# PRACTICE SHEET

## OBJECTIVE QUESTIONS

**1.** Advantage of synchronous sequential circuits over asynchronous ones is

(a) faster operation

(b) ease of a avoiding problems due to hazards

(c) lower hardware requirement

(d) better noise immunity

**2.** Which of the following is/are advantage of virtual memory?

(a) Faster access to memory on an average

(b) Processes can be given protected address spaces

(c) Linker can assign addresses independent of where the program will be loaded in physical memory

(d) Programs larger than the physical memory size can be run

**3.** The main differences(s) between a CISC and A RISC processor is/are that a RISC processor typically

(a) has fewer instructions

(b) has fewer addressing modes

(c) has more registers

(d) is easier to implement using hard-wired control logic

**4.** More than one word are put in one cache block to

(a) exploit the temporal locality of reference in a program

(b) exploit the spatial locality of reference in a program

(c) reduce the miss penalty

(d) None of the above

**5.** Which of the following is not a form of memory

(a) Instruction cache

(b) Instruction Register

(c) Instruction opcode

(d) Translation look aside buffer

**6.** Increasing the RAM of a computer typically improves performance because

(a) Virtual memory increases

(b) Larger RAMs are faster

(c) Fewer page faults occur

(d) Fewer segmentation faults occur

**7.** The memory locations 1000, 1001 and 1020 have data values 18, 1 and 16 respectively before the following program is executed.

```
MOVI    Rs,1            ; Move immediate
LOAD    Rd, 1000(Rs)    ; Load from memory
ADDI    Rd, 1000        ; Add immediate
STOREI  0(Rd), 20       ; Store immediate
```

Which of the statements below is TRUE after the program is executed?

(a) Memory location 1000 has value 20

(b) Memory location 1020 has value 20

(c) Memory location 1021 has value 20

(d) Memory location 1001 has value 20

**8.** Which of the following statements about relative addressing mode is FALSE?

(a) It enables reduced instruction size

(b) It allows indexing of array elements with same instruction

(c) It enables easy relocation of data

(d) It enables faster address calculations than absolute addressing.

**9.** Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in abit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively

(a) 256 Mbyte, 19 bits

(b) 256 Mbyte, 28 bits

(c) 512 Mbyte, 20 bits

(d) 64 Gbyte, 28 bits

## ANSWERS AND EXPLANATIONS

1. *Ans. (a)*

Synchronous sequential circuits has less dealy, therefore, synchronous circuits have faster operation than asynchronous ones.

2. *Ans. (d)*

Virtual memory is a concept which allows programs larger than the physical memory size to run.

3. *Ans. (a), (b), (c), (d)*

The major characteristics of a RISC processor are:

(a) Relatively few instructions.

(b) Relatively few addressing modes

(c) More registers

(d) Hardwaired rather than micropro-grammed control.

4. *Ans. (b)*

5. *Ans. (c)*

An opcode is the portion of a machine language instruction that specifices the operation to be performed.

6. *Ans. (c)*

Increasing the RAM means increase the primary memory which reduce the swapping so fewer page faults occur.

7. *Ans. (d)*

Content of register as program will be execute are

$R_0 = L$

$R_d$ = content of 1000(1) = 1000 + 1 = 10001 memory address

$\therefore \ R_d = 1$

$R_d$ = content of 1000(1) = 1000 + 1 = 1001 memory address

Add I. $R_{d'}$ 1000

$\therefore \ R_d = 100$

store 0 (1001), 20 means store 20 in the address value 1001.

8. *Ans. (b)*

It does not allow indexing of array element with same instruction.

9. *Ans. (a)*

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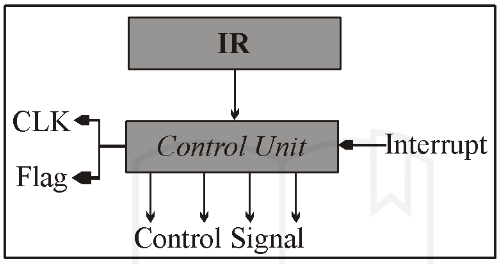
# CONTROL UNIT AND I/O

## THEORY

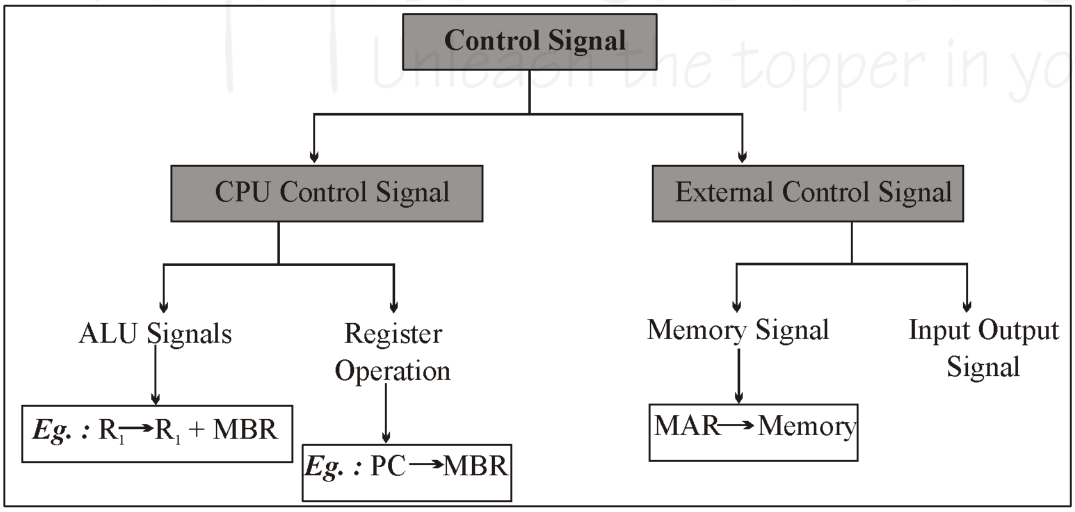
### INTRODUCTION



Control unit may have many input like IR (Instruction register), clock, flag, interrupt but the only output generation of the control singlas.

### 2.1 CONTROL SIGNALS

The control signals are calssified into two categories.



### 2.2 CONTROL UNIT IMPLEMENTED

This control unit can be implemented in two ways namely.

- Hardwired Control Unit
- Micro Programmed Control Unit

  ***Or*** Software Control Unit

### 2.2.1 Hardwired Control Unit :

It is very complex and combinational circuit, made up with NAND and NOR gate.

***Advantage :*** Very high speed.

***Disadvantage :***

- Very expensive
- It doesn't support new instruction
- Modifications are difficult
- Less flexility

***Example :***

| | $T_1$ | $T_2$ | $T_3$ |
|---|---|---|---|
| $I_1$ | $R_1$ in .mout | $R_2$ out min | $R_3$ in $R_1$ out |
| $I_2$ | Min. $R_1$ in | Mout $R_5$ in | $R_1$ in |
| $I_3$ | Mout $R_2$ out | PC out MA Rin | $R_2$ out |

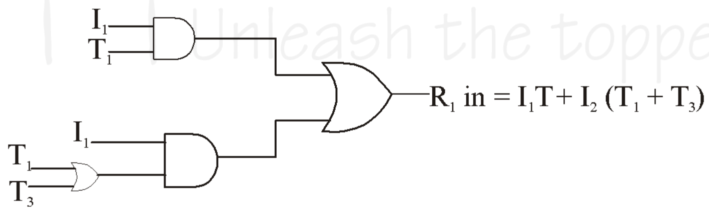
Write the operation for $R_1$ in and M out, min

***Solution:*** $R_1$ in $= I_1T_1 + I_2T_1 + I_2T_3$

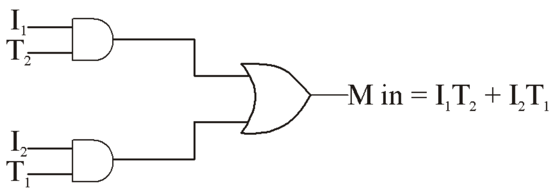
$$\boxed{\text{Rin} = I_1T_1 + I_2(T_1 + T_3)}$$

$$\boxed{\text{min} = I_1T_2 + I_2T_1}$$

***Hardware Implementation of $R_1$ in***



Hardware Implementation of M in

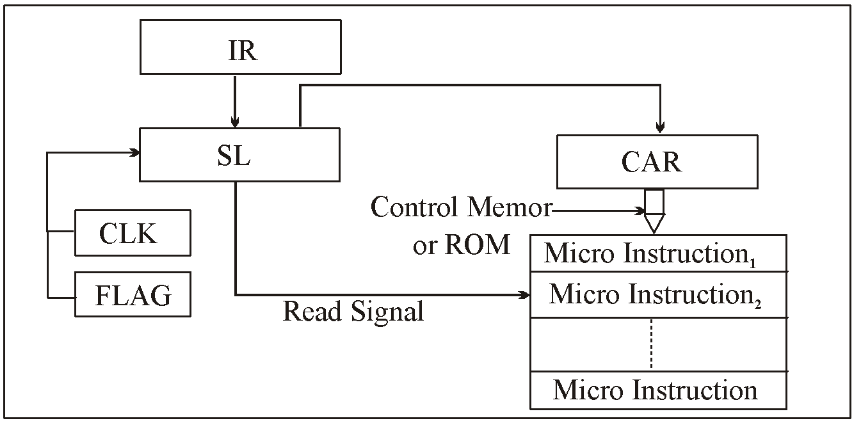


### 2.2.2 Microprogrammed Control Unit / Software Control Unit :

Difficulties of hardware control unil overcome with micro programmed control unit.

In which the control signals are generated by execution of microprogram.

Microprogram is a low level program written in 0's and 1's or set of instruction.



- IR (Instruction Registor)
- SL (Sequence Logic)
- CAR (Control Address Register)
- CBR (Control Buffer Register)

  ***Advantage :***

  - More flexible
  - Cheaper
  - Support new instruction

***MICRO INSTRUCTION FORMAT :***

| | | | | |
|---|---|---|---|---|
| 1. Control Field | 2. Control Field | ................................ | Flags | Next Micro Instruction Address |

***Control Field :*** It generate the control signals.

***Flags :*** They record the states of previous operation.

***Next micro Instruction Address :*** It determine the memory size.

## *TYPES OF MICRO INSTRUCTIONS :*

Micro instructions are classified into two categories.

***(i) Horizontal Micro Instruction :***

Horizontal micro instruction will have a long instruction format.

In which if we have n bit control field then total no of control instruction are n.

It doesn't require any encoding and decoding technique.

***Control Field :*** If we have n bit control field then total no of control signals. are n.

***Flag :*** If we have $2^n$ flags then we require n bit.

***Next Micro Instruction :*** If we have n bits for next micro instruction addressing then memory size = $2^n$.

***(ii) Vertical Micro Instruction :***

In which we require an additional circuit which is known as decoder.

It has short instruction format, if we have total $2^n$ control signal then control field have n bits.

***Control Field :*** Control field size = n bits than total control signals = $2^n$.

***Flag field :*** Flag field size = n bits then total no of flags = $2^n$.

**NEXT MICRO INSTRUCTION :**

***Address :*** If we have n bit for addressing then memory size $2^n$.

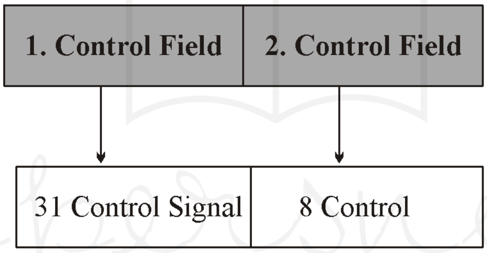
***Conparisison between hardwared and softwired control unit design.***

- ***Speed :*** Vertical < Horizontal < Hardwired
- ***Cost :*** Vertial < Horizontal < Hardwired.
- ***Time Consumption :*** Vertical > Horizontal > Hardwired
- ***Flexiblity :*** Hardwire < Horizontal < Vertical

Vertical micro-programmed control unit design technique require an additional decoder so speed is low, cost is high.

***Example :*** A micro control Instruction have two micro operations field. One field may generate one or upto 31 control signals field-2 suppose to generate one of 8 control signal. Find the min no of bits required to design control instruction.

***Solution:*** We require min no of bits for design a contol instruction so this can be possible by using vertical softwired control design.



So 5 bits are, r equired for field 1 and field 2 require 8 bit so minno of bits to design a control instruction = 5 + 3 = 8 bits

***Example :*** A micro program control unit is suppose to generate 48 control signals. If the control Instruction format given as:

| Flags | Micro Control Signal | Next Micro Instruction Address |
|---|---|---|

Find the control memory size in bytes if 8 flags conditions are used and control memory size 1024 words.

***Solution:*** There are two possiblies fordeter mining the size of memory

(1) By using horizonal micro-programmed method

(2) By using vertical micro-programmed method

(1) ***Horizontal micro-programmed method :*** By using horizontal softwired method.

48 control signal = 48 bits

8 flags = $2^3$ = 3 bits

Next instruction address = 1024 = $2^{10}$ = 10 bits

total no of bits required for = 48 + 3 + 10

= 61 bit , one word size

$$\frac{61}{8} = 7.625 \text{ byts}$$

We have total 1024 word

memory size = 1024 × 7.625 = 7808 byts

***If we use vertical micro-programmed technique :***

48 control signal = 6 bits

6 flags = $2^3$ = 3 bits

next instruction address = 1027 = $2^{10}$ = 10 bits

total no of bits = 19 bits

$$= \frac{19}{8} = 2.375 \text{ byts, one word}$$

total memory size = 1024 × 2.375 = 2432 byts.

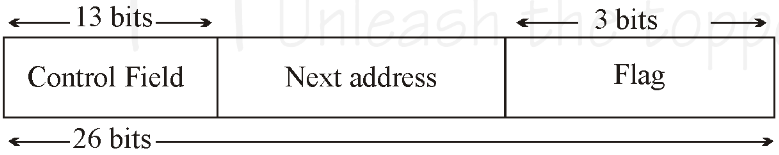
***Example :*** The micro instruction store in the control memory of a processor have a width of 26 bits each micro instruction is divided into 3 fields

field$_1$ = micro operation of 13 bits

Assume that there are 8 flags. How many bits are there is in *x* field and *y* fields and what is the size of control memory in no of words.

(a) 10, 3, 1024 (b) 8, 5, 256 (c) 5, 8, 2048 (d) 10, 3, 512

***Solution:*** **Ans. (a)**



So next address field bits = 26 – (13 + 3) = 10

Then total no of words = $2^{10}$ = 1024 words memory.

***Example :*** A hardwired CPU uses 10 control signals $S_1$------$S_{10}$, in various time stamps $T_1$, $T_0$, $T_5$ and implement 4 instructions $I_1$ to $I_4$ as follows

| | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_5$ |
|---|---|---|---|---|---|
| $I_1$ | $S_1, S_3, S_5$ | $S_2, S_4, S_6$ | $S_1, S_7$ | $S_{10}$ | $S_3, S_8$ |
| $I_2$ | $S_{17}, S_3, S_5$ | $S_8, S_9, S_{10}$ | $S_5, S_6, S_7$ | $S_6$ | $S_{10}$ |
| $I_3$ | $S_1, S_3, S_5$ | $S_7, S_8, S_{10}$ | $S_2, S_6, S_7$ | $S_{10}$ | $S_1, S_3$ |
| $I_4$ | $S_{17}, S_3, S_5$ | $S_2, S_6, S_7$ | $S_5, S_{10}$ | $S_6, S_9$ | $S_{10}$ |

Obtain the logic Function to generate $S_S$ and

***Solution:***

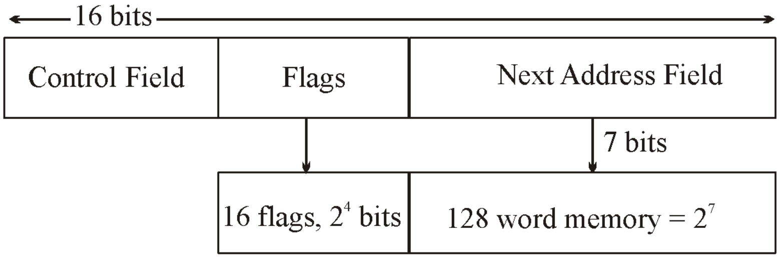
$$S_s = (I_1 + I_2 + I_3 + I_4)\ 8.\ T_1\ (I_2 + I_4)\ T_3$$

$$S_s = T_1 + (I_2 + I_4)\ I_3$$

$$S_{10} = (I_2 + I_3)\ T_2 + I_4\ T_3 + (I_1 + I_3)\ T_4 + (I_2 + I_4)\ T_5$$

***Example :*** 16 Bit micro instruction support, 16 conditions flags and stored in 128 word memory. What will the no of control signal signal generation in Horizontal and vertical softwired CU design.

***Solution:*** Horizontal



So we have = 16 – (4 + 7)

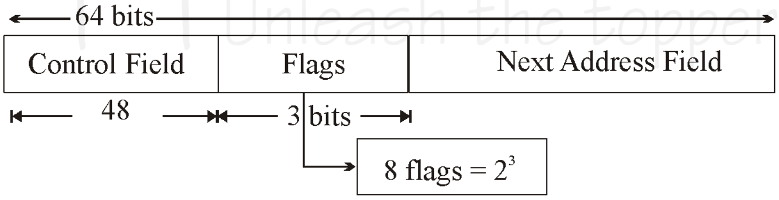
= 16 – 11 = 5 bits for control field

So total no of control signal = 5

In vertical micro-programmed CU design we have S bits for contrat field than $2^5 = 32$ control signals.

***Example :*** Consider a control unit design in which 48 control signals are to be genrated and the system support 8 flag conditions. If the 64 bit control word is store in memory then for horizental software control unit design technique determine the size of memory in byts and also for vertical softwared.

***Solution:***



So next address field = 64 – (48 + 3)

= 64 – (51)

= 13 bits

So the memory size in word = $2^3$

= 8192 words

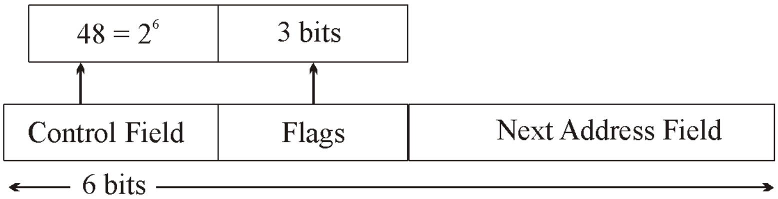
onew word size is given = 64 bits

memory size in bits = 8192 × 64 = 524288

in byte = 65536 byts = $2^{16}$ byte = $2^6 2^{10}$ byts

= 64 KB ***Ans.***

*Vertical micro-programmed CU Design :*



Next address field = 64 – (6 + 3) = 55 bits

Total = $2^{55}$ words = 64 × $2^{55}$ bits

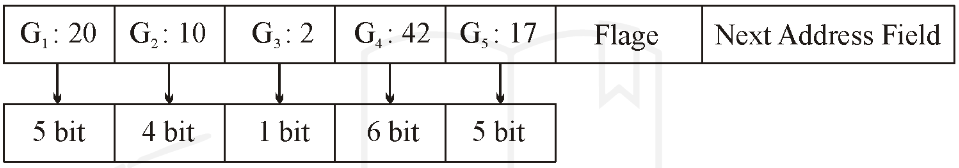
Size = 8 × $2^{55}$ byte of memory

***Example :*** A micro instruction supports 5 mutually exclusive group of control signal signal

$G_1$ : 20, $G_2$ : 10, $G_3$ : 2, $G_4$ : 42 and $G_5$ : 17

How many bits are saved using vertical CUD esignd over Horizental CUD.

***Solution:***



In horizontal = 20 + 10 + 2 + 42 + 17 = 91 bits

In vertical = 5 + 4 + 1 + 6 + 5 = 21 bits

= 91 – 21 = 70 bits are saved.

## <u>2.3 INPUT / OUTPUT INTERFACING</u>

Input/output interfacing is a machanism to access the data from the memory or write the data to the memory location by input/output devices is known as input/output interfacing.

There are three types of input/output interfacing

1. Programmed input/output
2. Interrupt Driven input/output
3. DMA transfer

### 2.3.1 Programmed Input / Output :

It is also known as programmed driven Input/output.

In this mode the Input/output has no direct access to main memory.

Each Input/output devices have a particular status register for performing the read from the memory or write to the memory.

So the processor periodically varify the status register when the status register become 1 then processor provide the Input/output permission to the respective device.

It is an inefficient mode of transfer :

*(1) Advantage :* Easy to implement

*(2) Disad Vantage :* Most of the CPU time wasted due to scanning the status register.

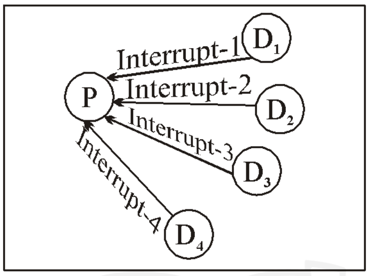
This technique suitable for limited data transfer.

It support only one operation at a time.

In which processor sit ideal until status Register = 1.

### 2.3.2 Interrupt Driven Input/Output :

*Initiated Input/output*



In this mode when the devices is ready, it send an interrupt to the processor for access the data from main memory.

In this technique micro processor will not sit ideal as programmed Input/output.

It performs some other task intile an interrupt signal received from Input/output interface so that this is a technique which provides the offective uitilization of CPU.

When CPU received and interrupt signal from Input/output devices then it stop the another operation and execute ISR ***(Interrupt Service Routine.)***

**DISADVANTAG :**

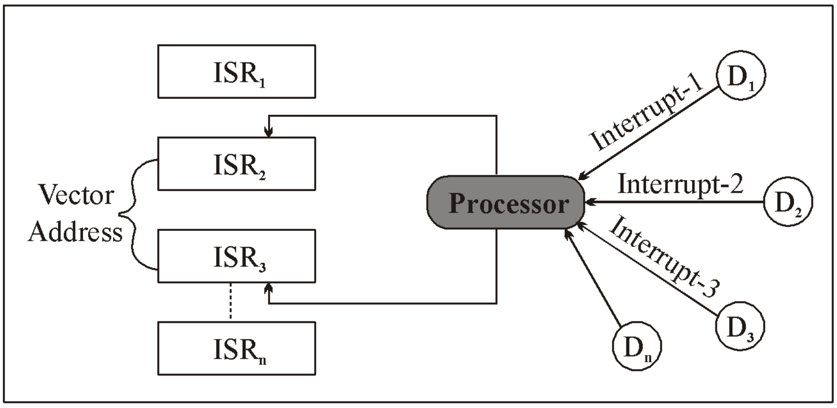
Not suitable for large valume of data transfer.

It more then one device interrupts simultaneously then priority driven Input/output is used.

Using this the high priority devices address (***vector address***) can be obtained.

So a device which have highest priority is access the data first and the address of this Input/output device is known as ***vector address.***

***(i) Software Approach or Software Polling :***

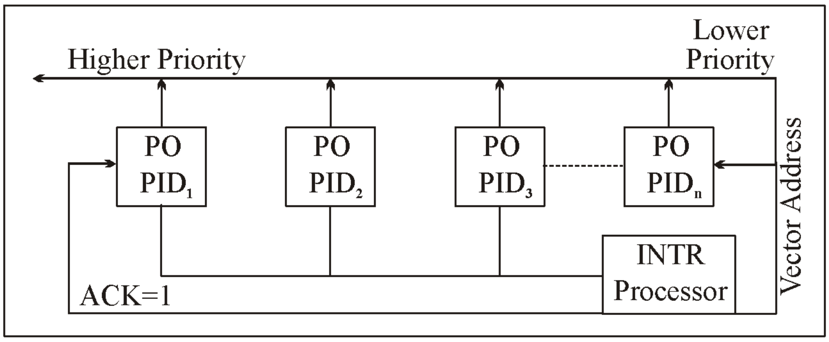


Executing a set of routines or data transfer is in efficient. Hence not recommended.

***(ii) Hardware Approach :***

In the hardware approach we have two types :

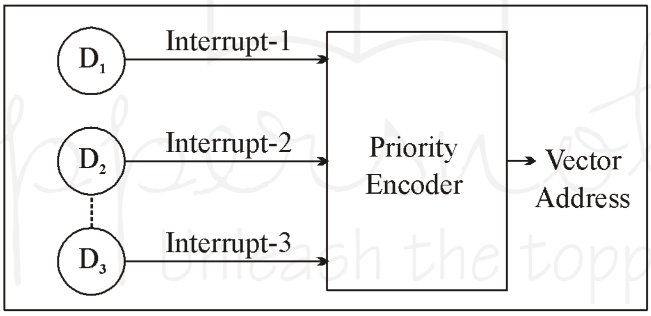
***(a) Serial / Daisy chain/Hardware Polling :***



So in the serial interrupt driven input output when all the devices generate the interrupt for getting permission for accessing the data from main memory, then we determine the vector address (highest priority devices address).

So CPU sends an acknowledgement to the vector address decice and the respective device perform input/output operation.

***(b) Parallel priority Driven Input/output***

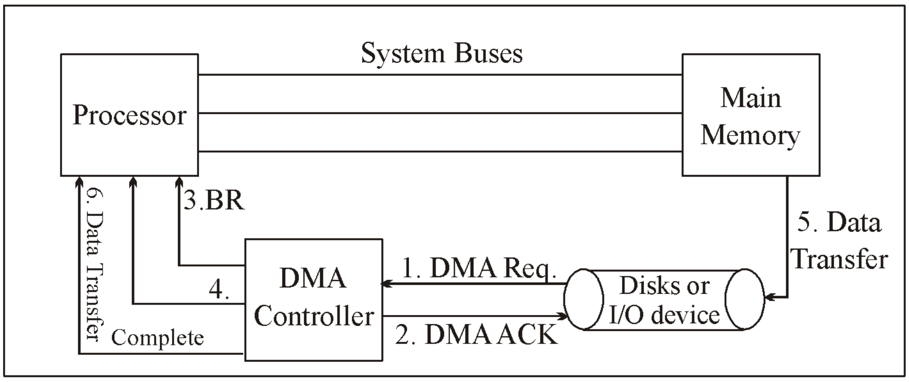


### 2.3.3 DMA (Direct Memory Access) :

This technique is used for transformation of the data between input/output devices and memory with out CPU intervention.

This method is suitable for bulky data transformation between input/output and memory.

This technique required special controller called ***DMA controller*** along with input/output interface.



So if a disk ordevice want to access data diroctly from the main memory then it sends a DMA reqired to DMA controller.

And DMA controller sents and ACK to the input/output devices.

Then DMA sends the BR (Bus Request) to CPU. Then processor grant the bus to DMA controller.

In the DMA CPU handover the following information to the DMA controller Instead of input/output interface.

(1) Address of the input/output devices

(2) Operation to be performed.

(3) Starting address of the memory location.

(4) The no of memory words to be transfered.

Once DMA received this information, DMA completes entire task with out CPU envalvement and DMA interact with CPU after end of the operation.

***(i) DMA Trafer Mode :***

Both CPU and DMA used the main memory for access the data but they used single data bus so data is colloided or JAM.

So there are three thransfer mode.

***(a) Inter Leaved Mode :***

In this mode the bus cycle devided into two half cycles.

Such that first half cycle accessed by CPU and second half cycle accessed by DMA.

***(b) Burst Mode :***

In this approach DMA access the bus whenever CPU do not use the bus.

***CPU priority > DMA prority***

***(c) Cycle Stealing Mode :***

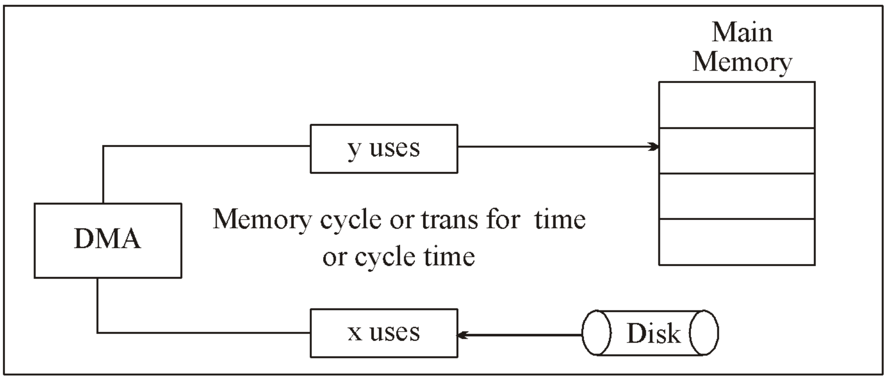
When CPU and DMA computer for bus access, DMA have right to suspend work of the CPU and steats the bus cycle from the CPU.

***CPU Prority < DAM Priority***

***(d) Block Mode :***

In the block mode DMA returns the bus after a block transfer.

***(ii) Some percentage performence is reduce due to DMA :***


Main Memory
y uses
DMA
Memory cycle or trans for time or cycle time
x uses
Disk